Special Trigger Algorithm

26th November 2003

Input Bits

Input Channel	Bit Description
0	Bits 0:2 – detector 0 special trigger request Bit 3 – unused Bits 4:6 – detector 1 special trigger request Bit 7 – unused Bits 8:10 – detector 2 special trigger request Bit 11 – unused Bits 12:14 – detector 3 special trigger request Bit 15 – unused
1	Bits 0:2 – detector 4 special trigger request Bit 3 – unused Bits 4:6 – detector 5 special trigger request Bit 7 – unused Bits 8:10 – detector 6 special trigger request Bit 11 – unused Bits 12:14 – detector 7 special trigger request Bit 15 – unused
2	Bits 0:2 – detector 8 special trigger request Bit 3 – unused Bits 4:6 – detector 9 special trigger request Bit 7 – unused Bits 8:10 – detector 10 special trigger request Bit 11 – unused Bits 12:14 – detector 11 special trigger request Bit 15 – unused
3	Bits 0:2 – detector 12 special trigger request Bit 3 – unused Bits 4:6 – detector 13 special trigger request Bit 7 – unused Bits 8:10 – detector 14 special trigger request Bit 11 – unused Bits 12:14 – detector 15 special trigger request Bit 15 – unused
4	Unused
5	Unused
6	Unused
7	Unused

Registers

Register	Register Description
0	16 LSB of 32-bit Zero-Bias prescale
1	16 MSB of 32-bit Zero-Bias prescale
2	12 LSB of 24-bit random bit generator rate
3	12 MSB of 24-bit random bit generator rate
4:12	Unused

13	1-bit command to latch current value of clock counters
14	12 LSB of 24-bit clock counter
15	12 MSB of 24-bit clock counter

Output Bits

Bit	Description
Bits 0:2	Copy of 3-bit special trigger request from selected detector or “000” if there is no special trigger request
Bits 3:6	4-bit number encoding which of detectors 0 to 15 is making the request
Bits 7:13	Unused
Bit 14	Zero-bias bit
Bit 15	Random bit
Bits 16:31	Unused

Internal Logic

- The special trigger requests are searched. If detector 0 is making a request then it is selected. If detector 0 is NOT making a request and detector 1 IS making a request then the request of detector 1 is selected. If neither detectors 0 or 1 are making requests then any request from detector 2 is selected, etc….
- The selected request is passed on to the last DSM along with a 4-bit number specifying which of the 16 possible detectors is making the request. If there are no requests then the output is set to zero.
- When the DSM is put into RUN mode the 24-bit clock counter starts from 0 and increments by 1 every tick of the RHIC clock.
- When the user writes to register 13 the current value of the clock counter is copied into registers 14, the 12 LSB, and 15, the 12 MSB, which can then be read out by the user.
- If a non-zero value is set for the zero-bias prescale (Reg. 0 and 1) then a counter starts from the prescale value and decrements by 1 every tick of the RHIC clock. When the current value of the counter reaches 1 the zero-bias bit is set, and the counter is reset to the starting value specified in the prescale registers.
- If a non-zero value is set in the random generator registers (Reg. 2 and 3) then the random bit generator is started. The register values are used to set the rate of exponential decay of a 32-bit number. When this number drops below a threshold value, chosen from a 128-bit linear feedback shift register, the random output bit is set. At this point the decaying number is reset to its maximum (all bits high) and a new threshold value is chosen from the shift register.